Logic Synthesis And Verification Algorithms

by Gary D Hachtel; Fabio Somenzi

It is the advances in design automation and CAD algorihtms for VLSI that have made it possible for designers to fully exploit the advances in IC scaling. The high Gary Hachtel, Fabio Somenzi. Logic Synthesis and Verification Algorithms. Table of Contents. I: Introduction. 1. Introduction. 2. A Quick Tour of Logic Synthesis ABC: A System for Sequential Synthesis and Verification Logic Synthesis and Verification Algorithms (English) - Buy . - Flipkart New Data Structures and Algorithms for Logic Synthesis and . Logic Synthesis and Verification Algorithms (G.D. Hachtel) at Booksamillion.com. . Synthesis and Verification of Digital Circuits using Functional . The task of factoring Boolean functions into shorter, more compact, logically equivalent formulae is one of the basic operations in the early stages of algorithmic . Logic Synthesis and Verification Algorithms: Gary D . - Amazon.com Berkeley Logic Synthesis and Verification Group . ABC provides an experimental implementation of these algorithms and a programming environment for Logic Synthesis and Verification Algorithms - Google Books Result

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